ABSTRACT OF THE INVENTION

A peripheral or memory device has a bus, a first bus decoder circuit coupled to the bus for decoding a first type of bus signal, and a second bus decoder circuit coupled to the bus for decoding a second type of bus signal. The device also includes a circuit for detecting whether the bus is a first type of bus or a second type of bus, and outputting a select or detect signal to a switch. The switch is coupled to the first bus decoder circuit for providing a first bus enable signal thereto, and the switch is coupled to the second bus decoder circuit for providing a second bus enable signal thereto, depending on the nature of the select or detect signal.